What is claimed is:

1. A method for forming an electrically conductive layer having patterns for semiconductor devices, comprising the steps of:

providing a substrate;

forming an insulation layer on the substrate, the insulation layer having predetermined functional groups;

forming a patterned polymer layer having the patterns on the insulation layer;

etching the insulation layer in accordance with the patterns of the patterned polymer layer to create a patterned insulation layer;

stripping the patterned polymer layer to expose the patterned insulation layer;

treating the patterned insulation layer with a coupling agent reacting with the predetermined functional groups;

treating the patterned insulation layer with a catalyst-containing solution; and

depositing electrically conductive material on the patterned insulation layer.

2. The method of claim 1, wherein the predetermined functional groups include OH functional groups.

3. The method of claim 2, wherein the insulation layer is a silicon oxide (SiO_x) layer.

4. The method of claim 1, wherein the catalyst-containing solution includes a catalyst selected from the group including palladium (Pd), platinum (Pt), tin (Sn), nickel (Ni), and any alloy thereof.

5. The method of claim 1, wherein the insulation layer has a thickness between about 1 nm and about 10 nm.

6. The method of claim 1, wherein the patterned polymer layer is formed by photolithography or micro-contact printing.

7. The method of claim 1, wherein the patterned polymer layer has a thickness between about 50 nm and about 100 nm.

8. The method of claim 1, wherein the patterned polymer layer comprises solvent soluble polyimide.

9. The method of claim 1, wherein the catalyst-containing solution has a catalyst making a bonding reaction with the coupling agent.

10. The method of claim 9, wherein the catalyst-containing solution is

selected from the group including a Pd/Sn colloidal mixture, an aqueous solution of $PdCl_2$, and any mixture thereof.

11. The method of claim 9, wherein the step of treating the patterned insulation layer with the catalyst-containing solution includes making surfaces of the patterned insulation layer catalytically active, so that the electrically conductive material is deposited on the catalytically active surfaces of the patterned insulation layer.

12. The method of claim 1, wherein the coupling agent is a silane coupling agent, and the predetermined functional groups are OH functional groups.

13. The method of claim 1, wherein the electrically conductive material is selected from the group including copper, silver, palladium, nickel, cobalt, gold, platinum, and any alloy thereof.

14. The method of claim 1, further including forming a non-functional insulation layer on the substrate, so that the insulation layer having the predetermined functional groups is formed on the non-functional insulation layer.

15. A method for forming an electrically conductive layer having

patterns for semiconductor devices, comprising the steps of:

providing a substrate;

forming an insulation layer on the substrate, the insulation layer having predetermined functional groups;

forming a patterned polymer layer having the patterns on the insulation layer, the patterned polymer layer having a coupling agent;

etching the insulation layer in accordance with the patterns of the patterned polymer layer to create a patterned insulation layer;

stripping the patterned polymer layer to expose the patterned insulation layer;

treating the patterned insulation layer with a catalyst-containing solution; and

depositing electrically conductive material on the patterned insulation layer.

16. The method of claim 15, wherein the coupling agent in the patterned polymer layer reacts with the predetermined functional groups in the insulation layer.

17. The method of claim 16, wherein the coupling agent is a silane coupling agent and the predetermined functional groups are OH functional groups.

18. A semiconductor device comprising:

a substrate;

a patterned insulation layer formed on the substrate, the patterned insulation layer having predetermined patterns; and

a plating layer formed on the patterned insulation layer, the plating layer having electrically conductive patterns corresponding to the predetermined patterns of the patterned insulation layer,

wherein the patterned insulation layer has catalytically active surfaces, and the electrically conductive patterns are formed by depositing electrically conductive material on the catalytically active surfaces of the patterned insulation layer.

19. The semiconductor device of claim 18, wherein the surfaces of the patterned insulation layer are treated with a silane coupling agent and a catalyst-containing solution to become catalytically active.

20. The semiconductor device of claim 19, wherein the silane coupling agent makes a bonding reaction with catalyst in the catalyst-containing solution and functional groups in the patterned insulation layer.

21. The semiconductor device of claim 20, wherein the functional groups in patterned insulation layer are OH functional groups, and the catalyst

is selected from the group including palladium (Pd), platinum (Pt), tin (Sn), nickel (Ni), and any alloy thereof.